

FORM PTO-892 (REV. 2-92)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. <b>10-072,843</b>	GROUP ART UNIT <b>2817</b>	ATTACHMENT TO PAPER NUMBER <b>4</b>
NOTICE OF REFERENCES CITED				APPLICANT(S) <b>Sutardja</b>		

  

U.S. PATENT DOCUMENTS							
•	DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE	
	<del>A 560,000</del>						
	<b>B 6122131</b>	<b>9-19-2000</b>	<b>Jeppson</b>	<b>360</b>	<b>77.02</b>		
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

  

FOREIGN PATENT DOCUMENTS									
•	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SMTS. DWG	PP SPE	
	<b>L 061752</b>	<b>3-4-1994</b>	<b>Japan</b>	<b>Matsuyama et al.</b>	<b>330</b>	<b>308</b>			
	M								
	N								
	O								
	P								
	Q								

  

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)	
R	<b>You et al. "A multistage amplifier topology with nested Gm-C compensation for low-voltage application" IEEE International Solid-State Circuits Conference, 1997 Digest of Technical Papers, 44<sup>th</sup> ISSCC February 6-8, 1997 pp 348-349</b>
T	<b>Holt "Electronic Circuits Digital and Analog" John Wiley &amp; Sons 1978 pp 423, 431, 436</b>
U	

  

EXAMINER <b>MICHAEL B. SHINGLETON</b>	DATE <b>3-8-2003</b>	<b>1</b>
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\* A copy of this reference is not being furnished with this office action.  
(See Manual of Patent Examining Procedure, section 707.05 (a).)